[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **REPLY BRIEF IN SUPPORT OF PLAINTIFFS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER** **[RELATED CASES]** **DATE: NOVEMBER 30, 2012** **TIME: 10:00 A.M.** **PLACE: COURTROOM 5, 4TH FLOOR** **JUDGE: PAUL SINGH GREWAL**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

I. INTRODUCTION

TPL's opposition papers (Dkt. 367 *Acer* Action, hereinafter "Opposition") employ the familiar refrain of accusing Plaintiffs of attempting to import extraneous limitations into the claims. ("TPL" includes Defendants Technology Properties Ltd., Patriot Scientific Corp. and Alliacense Ltd.) TPL's arguments are without merit, and Plaintiffs' proposed constructions should be adopted.

With respect to the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" from U.S. Patent No. 5,440,749 (the "'749 patent" or "'749"), TPL attempts to obfuscate the issue by accusing Plaintiffs of seeking to exclude any system that happens to include a prefetch buffer or a one-instruction-wide instruction buffer. But this is not and has never been Plaintiffs' position. TPL made clear and unmistakable disclaimers during the '749 reexamination in which it told the Patent Office that this phrase excludes systems that supply instructions to the CPU one at a time. Plaintiffs merely seek to hold TPL to its representations to the Patent Office, which were neither rescinded during the reexamination nor affected by subsequent amendments to other claim elements.

With respect to the phrase "clocking said central processing unit" in U.S. Patent No. 5,809,336 (the "'336 patent" or "'336"), the Court should adopt Plaintiffs' construction because clocking the CPU to always achieve its maximum speed was described, in both the specification and file history, as a feature of the invention and a distinction over the prior art. TPL suggests that the intrinsic record merely describes the ability of the CPU to sometimes operate at the fastest possible speed, but this is inconsistent with the intrinsic record and would recapture the prior art systems that were criticized and distinguished throughout the intrinsic record.

II. ARGUMENT

A. "SUPPLY THE MULTIPLE SEQUENTIAL INSTRUCTIONS . . . "

TPL's argument on this phrase begins with the misleading heading "Judge Ware Correctly Construed the 'Supply Multiple Sequential instructions . . . ' Phrase." (Defs.' Response Brief in Opposition to Plaintiffs' Motion for Reconsideration at 3:4–5 ("Opposition"), Dkt. 367, *Acer Inc. et al. v. Technology Properties Ltd. et al.*, 08-cv-877-PSG ("*Acer* Action") (capitalization

altered).) But Judge Ware did not construe this phrase at all. He specifically declined to construe it based on his erroneous belief that the sole issue tendered for decision was "whether the phrase should be defined as requiring a 'prefetch buffer.'" (First Claim Construction Order at 8, *Acer* Action, Dkt. No. 336 ("Order").) TPL implicitly acknowledges as much by advancing its own construction of this phrase, which is the same construction it pursued in its arguments before Judge Ware. The proper construction of this phrase is therefore properly before this Court.

1. TPL Misstates the Underlying Dispute.

TPL devotes a large portion of its argument on this phrase to refuting a supposed position of Plaintiffs that they have not actually taken—that this phrase excludes any system that has either a prefetch buffer or a one-instruction-wide instruction buffer. (Opposition at 4.) This is not and has not been Plaintiffs' position. Plaintiffs have instead argued for a construction of this phrase that excludes "a prefetch buffer or a one-instruction-wide instruction buffer that ***supplies one instruction at a time***." (*See id.* at 3 (Plaintiffs' Proposed Construction).) The key issue in this phrase is whether it excludes instructions being supplied to the CPU one at a time, regardless of the physical structure used to supply the instructions.

Plaintiffs' proposed construction refers to a "prefetch buffer" and a "one-instruction-wide instruction buffer" only because TPL expressly distinguished those structures in the prior art which were used to supply instructions one at a time to the CPU. For example, TPL made the following disclaimer in distinguishing Edwards:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a **one-instruction-wide instruction buffer**, one at a time, and are there decoded. Fetching multiple instructions into a **prefetch buffer** and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of "multiple sequential instructions to a CPU during a single memory cycle."

(Amendment, 1/19/2010, at 26 of 58, Chen Decl. Ex. 2, *Acer* Action, Dkt. No. 358-3 (emphasis added).)

TPL has no legitimate basis to object to the reference to a "prefetch buffer" or a "one instruction-wide buffer" in the proposed construction of this phrase. Plaintiffs' proposed construction would not exclude a system simply because it happens to include a prefetch buffer or

a one-instruction-wide instruction buffer. But it would exclude a system that uses one of those structures to supply instructions one at a time to the CPU.

TPL appears to concede, in fact, that it did disclaim a system that supplies instructions one at a time to the CPU. In characterizing its own arguments to the Patent Office during the '749 reexamination, TPL states that each of its statements:

> expressly distinguishes the prior art reference on the same basis: (1) the instructions are supplied to the CPU one at a time, (b) although two instructions might be fetched at the same time, one instruction is supplied to the CPU at a time, and (c) the 'during a single memory cycle' limitation is not satisfied by supplying only one instruction to the CPU at a time.

(Opposition at 5:26–6:2.)

But TPL's proposed construction of this phrase does not incorporate an express prohibition against supplying instructions one at a time to the CPU. Its construction, "provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle," merely parrots other language of the claim. Because TPL concedes that the claimed systems do not supply instructions to the CPU one at a time, Plaintiffs' construction should be adopted:

> provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time**

(Plaintiffs' Motion for Reconsideration at 2, *Acer* Action, Dkt. No. 358 (emphasis added).)

2. The Amendments to Claim 1 Did Not Rescind Earlier Disclaimers.

TPL relies on amended language at the end of claim 1, which recites that supplying the multiple sequential instructions to the CPU "comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched." ('749 *Ex Parte* Reexamination Certificate, 1:65–2:2, Chen Decl. Ex. 1, *Acer* Action, Dkt. No. 358-2).) TPL suggests that this amendment to claim 1 should be viewed as actually defining the disputed phrase, effectively erasing TPL's earlier disclaimers. (Opposition at 6.) This argument is without merit for at least two reasons.

First, TPL does not explain how any of its earlier disclaimers were rescinded or otherwise rendered ineffective. Although a disclaimer made during prosecution can be rescinded, "the prosecution history must be sufficiently clear to inform the examiner that the previous disclaimer, and the prior art that it was made to avoid, may need to be re-visited." *Hakim v. Cannon Avent Group, PLC*, 479 F.3d 1313, 1318 (Fed. Cir. 2007). This never happened during the '749 reexamination. TPL never informed the Examiner that its previous disclaimers made in distinguishing Edwards, May, and/or MacGregor needed to be revisited. And TPL never rescinded its earlier disclaimers.

Second and more fundamentally, the amendment to claim 1 does not even address the question of whether the phrase at issue here, "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," excludes systems that supply instructions one-at-a-time to the CPU. The amended language merely recites a ***sub-step*** to the process of supplying multiple sequential instructions to the CPU. This is apparent from the amended claim language, which states that supplying the multiple sequential instructions to the CPU "*comprises* supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle." ('749 *Ex Parte* Reexamination Certificate, 1:65–2:2, Chen Decl. Ex. 1, *Acer* Action, Dkt. No. 358-2 (emphasis added).) This language, using the open-ended "comprising" transitional phrase, does not ***define*** the claimed step of supplying the multiple sequential instructions to the CPU—it merely specifies a particular sub-step that the claim step must include.

The fact that the amendment represents merely a sub-step is evident from a critical difference between the language of the term being construed and the amendment to claim 1 that TPL has overlooked. The amended language of claim 1 recites "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle," while the phrase being construed is "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." As explained below, because TPL's amendment involves the "instruction register," not the separately claimed "central processing unit

integrated circuit" (CPU), it has no bearing on reexamination disclaimers directed specifically at the phrase at issue here.

The "instruction register" and the CPU ("central processing unit integrated circuit") are separate and distinctly recited components of the claimed microprocessor system. Claim 1, in particular, recites a "microprocessor system" that comprises a "central processing unit integrated circuit" (CPU) which, in turn, "include[es] an arithmetic logic unit and a first push down stack." (*Id.* at 1:43.) The claim does not list the "instruction register" as a component of the CPU. The claim instead recites "an instruction register" four elements later in the claim, as an element of the broader microprocessor system ("wherein the ***microprocessor system*** comprises an instruction register") (*id.* at 1:55–57 (emphasis added)), not as part of the earlier-recited CPU. It is well-settled Federal Circuit law that "[w]here a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Group, LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (quoting *Gaus v. Conair Corp.*, 363 F.3d 1284, 1288 (Fed. Cir. 2004)). Had the patentee intended for the "instruction register" to have been a part of the claimed CPU, it would have added that component to the CPU element rather than separately claiming it as part of the overall "microprocessor system."

Because supplying multiple sequential instructions to the "instruction register" as recited in the amendment does not by itself complete the step of supplying those instructions to the CPU, the amendment merely recites a sub-step in the process of supplying those instructions to the CPU. This is entirely consistent with the specification, which explains that the instructions must be supplied <u>from</u> the instruction register <u>to</u> the CPU. (*See* '749, 2:40–45 ("In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register ***for supplying the multiple instructions in succession <u>from</u> the instruction register***.") (emphasis added).)[1]

[1] To use a real-world analogy, a claim could recite that "a means for delivering documents to Judge Grewal's courtroom on the fourth floor comprises clearing security on the first floor of the

The "instruction register" amendments to claim 1 therefore have no relevance to TPL's disclaimers regarding the phrase at issue here, "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." TPL's disclaimers in the reexamination all related to supplying the instructions to the CPU, not to the instruction register. Those disclaimers did not even use the term "instruction register," let alone distinguish the prior art based on supplying the instructions to the instruction register.

3. Plaintiffs' Construction Will Prevent TPL's Improper Attempt To Recapture Disclaimed Subject Matter.

The importance of holding TPL to its statements to the Patent Office is highlighted by its Infringement Contentions as to the '749 patent seeking to accuse systems that behave in precisely the same way as the prior art distinguished during the reexamination. TPL's infringement contentions rely on a mode of operation in the accused systems ("Thumb mode") in which instructions are fed to the CPU one at a time. (Product Reports at 6 and 14 of 24, Chen Decl. Ex. 4, *Acer* Action, Dkt. No. 358-5 (emphasis added) (quoting ARM Ltd., An Introduction to Thumb).) TPL does not dispute that the accused products operate in this way, but contends that this is permissible because multiple instructions are received in parallel "by the instruction register." (Opposition at 8.) This argument relies on the assumption that the "instruction register" is part of the CPU, which is incorrect as explained above. Plaintiffs' proposed construction, which expressly excludes systems in which instructions are supplied to the CPU one at a time, must be adopted to prevent TPL's improper attempt to recapture the systems that it disclaimed to overcome prior art during the '749 reexamination.

B. "CLOCKING SAID CENTRAL PROCESSING UNIT"

The interpretation of the phrase "clocking said central processing unit" turns on whether TPL's emphatic statements in the specification and prosecution history describing the clocking of the invention should be given weight in claim construction. TPL attempts to characterize these statements as merely "describing one advantage of a preferred embodiment" (Opposition at 11),

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building at 280 South First Street." Clearing security on the first floor would certainly be a required sub-step in the delivery of the documents, but the delivery could not be complete until the documents were subsequently carried to Judge Grewal's courtroom on the fourth floor.

but this is inaccurate. The '336 specification and prosecution history describe the feature of always clocking the CPU at its maximum speed as a feature of the invention, and criticize prior art systems lacking this feature. This feature is properly incorporated into the construction of this term. *See, e.g.*, *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329–30 (Fed. Cir. 2009) ("Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.") (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001)).[2]

TPL repeats the same misleading argument it made to Judge Ware, that "[t]he specification of the patents-in-suit discloses multiple embodiments of the various inventions; so many that the PTO required the applicants to divide the original application into 10 separate applications." (Opposition at 11:13–15.) But those supposed "multiple embodiments" did not relate to the clocking mechanism claimed in the '336 patent. As explained in connection with TPL's own motion for reconsideration, the examiner issued a restriction requirement during the prosecution of the '749 patent directing the applicants to file separate divisional applications because the applicants' proposed claims covered distinct inventions (Group I through Group X). Only one of those so-called "multiple embodiments" (Group V) was directed to the clocking features of the disclosed microprocessor system. (08/31/1992 Restriction Requirement, at ¶ 19 (Group V), Chen Decl. Ex. 6, *Acer* Action, Dkt. No. 368-7.)[3]

The applicants were forced to file separate divisional applications because their claims were directed at "independent and distinct inventions," 35 U.S.C. § 121, not because they covered multiple embodiments of a single invention, as TPL now suggests. With respect to the clocking features of the disclosed microprocessor system, their entire detailed description is contained in a

[2] TPL misleadingly suggests that Judge Ward construed this phrase in the previous Texas litigation involving the '336 patent, but he did not. Judge Ward construed a narrower and different phrase directed to what an "oscillator" was, not how the CPU was clocked. (See Ward Order at 13, Otteson Decl. Ex. 3, *Acer* Action, Dkt. No. 357-3.)

few passages between columns 16 and 17 of the specification. ('336, 16:44–17:37, *Acer* Action, Dkt. No. 358-6). The "ring oscillator" described in those passages is the only disclosed embodiment for clocking the CPU.

1. TPL's Attempt To Recapture the Prior Art Should Be Rejected.

TPL argues that nothing in the specification or the prosecution history "requires the clock operate at the fastest possible speed; rather, the embodiment discussed merely allows the clock to operate at a fastest possible speed." (Opposition at 12:10-11 (emphasis in original).) This argument cannot be reconciled with the plain language of the specification, which states that "[b]y deriving system timing from the ring oscillator 430, CPU 70 will ***always*** execute at the maximum frequency possible, but never too fast." ('336, 16:63–17:2, Chen Decl. Ex. 5, *Acer* Action, Dkt. No. 358-6; *see also id.*, 17:19–21 ("The CPU 70 executes at the fastest speed possible using the adaptive ring counter[ ] clock 430.").)

But more fundamentally, a system that merely allows the CPU clock to operate at the fastest possible speed would recapture the prior art systems that TPL distinguished in the '336 specification and during prosecution. The specification explains that prior art CPUs were clocked at a "rated clock speed" to achieve best performance under worst case conditions. (*Id.*, 16:47–53.) Those prior art systems, therefore, ***will*** operate at the fastest possible speed ***under those worst case conditions***. (*See* Amendment, 1/13/97, at 3–4, Chen Decl. Ex. 8, *Acer* Action, Dkt. No. 358-9 ("In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operation conditions . . . . Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.").) Construing this phrase to merely allow the CPU to sometimes operate at its maximum frequency, therefore, would recapture indisputably disclaimed prior art systems.

The purported advantage of the alleged invention's use of an on-chip oscillator clock is that the clock "always" adjusts to maintain the same relationship with the CPU's maximum speed. If voltage, temperature, or other conditions cause the CPU's maximum speed to drop, these conditions "always" cause a corresponding change to the on-chip oscillator clock's frequency as well. ('336, 16:63–17:2, Chen Decl. Ex. 5, *Acer* Action, Dkt. No. 358-6.) The construction of

"clocking said CPU" must therefore not merely allow, but require, that the CPU always execute at the maximum frequency possible.

2. Plaintiffs' Proposed Construction Is Not Vague or Ambiguous.

TPL asserts that Plaintiffs' construction that the CPU "will always execute at the maximum frequency possible, but never too fast" is vague and ambiguous. (Opposition at 13.) TPL further asserts that the construction specifies no criteria to enable a jury to determine the "maximum frequency possible" or whether the CPU is going "too fast." TPL's own statements, however, debunk such an assertion. TPL had no trouble at all understanding the "fastest speed possible" (*i.e.*, "maximum frequency possible") of the CPU to mean "the upper end of the range of speeds at which the CPU can operate." (*See* Pls.' Claim Construction Brief at 24, *Technology Properties Ltd. et al. v. Fujitsu et al.*, 05-cv-00494-TJW, Dkt. No. 220 (Supplemental Decl. of Kyle Chen in Support of Motion for Reconsideration, Ex. 10).) Citing its own expert declaration, TPL further explained that the fastest speed possible is "the maximum frequency a CPU can operate at and still provide a valid output." (*Id.*) TPL even explained that, when "the frequency of a CPU exceeds its maximum theoretical performance," *i.e.*, when the frequency is "too fast," "errors are likely to result." (*Id.*) TPL thus has no basis to argue that a construction based on the applicants' own statements in the specification and prosecution history is either vague or ambiguous.

III. CONCLUSION

For the foregoing reasons, Plaintiffs' motion for reconsideration should be granted in its entirety.

Dated: November 9, 2012

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ATTESTATION PER GENERAL ORDER 45

I, Kyle D. Chen, am the ECF User whose ID and password are being used to file Corrected Plaintiffs' Consolidated Opening Supplemental Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

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